NON-MICROPIPE DISLOCATIONS IN 4H-SiC DEVICES: ELECTRICAL PROPERTIES AND DEVICE TECHNOLOGY IMPLICATION

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ABSTRACT

It is well-known that SiC wafer quality deficiencies are delaying the realization of outstandingly superior 4H-SiC power electronics. While efforts to date have centered on eradicating micropipes (i.e., hollow core super-screw dislocations with Burgers vectors > 2c), 4H-SiC wafers and epilayers also contain elementary screw dislocations (i.e., Burgers vector = 1c with no hollow core) in densities on the order of thousands per cm^2, nearly 100-fold micropipe densities. While not nearly as detrimental to SiC device performance as micropipes, it has been previously shown that diodes containing elementary screw dislocations exhibit a 5% to 35% reduction in breakdown voltage, higher pre-breakdown reverse leakage current, softer reverse breakdown I-V knee, and concentrated microplasmic breakdown current filaments when measured under DC testing conditions. This paper details the impact of elementary screw dislocations on the experimentally observed reverse-breakdown pulse-failure characteristics of low-voltage (< 250 V) small-area (< 5 x 10^{-4} cm^2) 4H-SiC p^+n diodes. The presence of elementary screw dislocations did not significantly affect the failure properties of these diodes when subjected to non-adiabatic breakdown-bias pulsewidths ranging from 0.1 μs to 20 μs in duration. Diodes with and without elementary screw dislocations exhibited positive temperature coefficient of breakdown voltage and high junction failure power densities well above the failure power densities exhibited by highly reliable silicon power rectifiers. This preliminary result, based on measurements from one wafer of SiC diodes, suggests that highly reliable low-voltage SiC rectifiers may be attainable despite the presence of elementary screw dislocations.

INTRODUCTION

It is widely recognized that material quality deficiencies are the primary reason why SiC high-power devices cannot be realized at present. While small-current, small-area high-voltage (1-5 kV) SiC devices are being prototyped and tested, the high densities of crystallographic defects in SiC wafers prohibits the attainment of SiC devices with very high operating currents (> 50 A) that are commonly obtainable in silicon-based high-power electronics [1, 2]. Micropipe defects are clearly very detrimental to electrical device performance, as these defects cause premature breakdown point-failures in SiC high-field devices fabricated in 4H- and 6H-SiC c-axis crystals with and without epilayers [2]. Commercial 4H- and 6H-SiC wafers and epilayers also contain elementary screw dislocations (i.e., Burgers vector = 1c with no hollow core) in densities on the order of thousands per cm^2, nearly 100-fold micropipe densities [3-6]. Because of the non-terminating behavior of screw dislocations, both hollow-core (micropipes) and non-hollow-core (elementary) screw dislocations and associated crystal lattice stresses are replicated in subsequently grown SiC epilayers [7, 8].

The electrical impact of elementary screw dislocation defects on SiC device performance has largely been overlooked while attention has focused on eradicating SiC micropipes. However, as SiC micropipe densities fall below 1 per cm^2 in the best reported wafers [9], the operational effects of elementary screw dislocations must now be considered. While not nearly as detrimental to SiC device performance as micropipes, it has recently been demonstrated that elementary screw dislocations somewhat degrade the reverse leakage and breakdown properties of 4H-SiC p^+n diodes [10]. Diodes containing elementary screw dislocations exhibited a 5% to 35% reduction in breakdown voltage, higher pre-breakdown reverse leakage current, softer reverse breakdown I-V knee, and highly localized microplasmic breakdown current filaments.

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Localized breakdowns and high-current filaments at junction hotspots are undesirable in silicon-based solid-state power devices. In operational practice, silicon power devices that uniformly distribute breakdown current over the entire junction area exhibit much greater reliability than silicon devices that manifest localized breakdown behavior. This is because silicon devices that avoid localized junction breakdown exhibit larger Safe Operating Areas (SOA's) and can much better withstand repeated fast-switching stresses and transient overvoltage glitches that arise in high-power systems [11-14]. Positive temperature coefficient of breakdown voltage (PTCBV), a standard behavior in silicon power devices free of crystal dislocation defects, helps insure that current flow is distributed uniformly throughout a device, instead of concentrated at high-current filaments. This enables silicon power rectifiers to exhibit a high energy to thermal junction failure when subjected to transient breakdown or switching bias conditions in which voltage and current are simultaneously large in the device. It is generally accepted that power rectifier SOA and reliability increases with increasing semiconductor junction energy to fail. Silicon junctions that suffer localized breakdown due to the presence of crystal dislocation defects do not generally exhibit sufficient energy to fail characteristics to be considered reliable for use in high-power systems.

Before SiC can become feasible for widespread incorporation into high-power systems, SiC power devices must demonstrate at least equal, if not superior, reliability characteristics as present-day dislocation-free silicon power devices. Therefore, SiC power devices must demonstrate at least equal, if not superior, SOA's and immunity to switching and overvoltage stresses as silicon power devices. Since all appreciable current (> 1 A) SiC power devices are virtually guaranteed to contain elementary screw dislocations, it is important to ascertain the junction breakdown and energy-to-fail characteristics of SiC diodes with elementary screw dislocations. The study reported in this paper quantitatively compares (to first order) theoretical and experimentally measured energy-to-fail characteristics of 4H-SiC p^+n junction diodes, with and without screw dislocations, to the well-known failure characteristics of silicon diodes.

SILICON AND SILICON CARBIDE JUNCTION FAILURE THEORY

One method of measuring diode junction failure characteristics is to subject the device to high-voltage pulses that momentarily bias the device beyond its reverse breakdown voltage. As high breakdown current is drawn at high applied voltage, a large breakdown power is dissipated at the junction which quickly heats up the device. Pulses of increasing amplitude or duration are applied until a critical junction failure temperature T_m is reached, at which point the device is unrecoverably damaged. For short pulse durations between 0.1 μs and 20 μs in length, heat flow occurs almost exclusively from the active device junction into bulk semiconductor wafer substrate; heat flow from the substrate to the package is essentially negligible on this timescale. Wunsch and Bell [15] derived a general first-order approximation for the junction power density P_D (kW/cm^2) applied over time t (μs) necessary for a device to reach a critical failure temperature T_m from an initial starting temperature of T_i:

$$P_D = \sqrt{\pi \kappa \rho C_p}\left[T_m - T_i\right] t^{-1/2} \text{ kW/cm}^2 \qquad (1)$$

where κ is the thermal conductivity (W/cm-K), ρ is the density (g/cm^3), and C_p is the specific heat of the semiconductor (J/gm-K). One choice for T_m is the temperature at which intrinsic carriers exceed the junction doping leading to second breakdown [11]. Metal-semiconductor contact degradation can also limit the peak temperature a device can withstand without damage. For more general first-order calculations that are independent of the junction doping and contact metallization, T_m is often set to the semiconductor Debye temperature T_D. The theoretical P_D vs. t curve calculated by Wunsch and Bell [15] for silicon using ρ = 2.33 g/cm^3, C_p = 0.7566 J/gm-K, κ = 0.526 W/cm-K, T_i = 298 K, $T_m = T_D$ = 948 K is:

$$P_D = 1109\ [t\ (\mu s)]^{-1/2} \text{ kW/cm}^2 \qquad \{\text{Silicon Theoretical}\} \qquad (2)$$

Wunsch and Bell found that (1) reasonably approximates the general junction failure behavior of a wide variety of experimental silicon rectifiers. However, the experimentally observed best fit to the P_D vs. t curve they observed for silicon rectifier diodes actually followed the relation [15]:

$$P_D = 560\ [t\ (\mu s)]^{-1/2}\ kW/cm^2 \qquad \{Silicon\ Experimental\} \qquad (3)$$

which lies somewhat below the theoretical calculation (2). Silicon experimental studies also indicate that pulse shape does not significantly change experimental device failure power densities, so that average power density may be used as a good approximation when diode voltage and/or current waveforms are non-constant over the pulse duration [14].

If current flow is focused through junction hotspots or defects, the effective power density, which is normalized to the total junction area instead of the hotspot junction area, will decrease accordingly. For example, if current flow is focused through hotspots so that most of the current flows through only 10 % of the total junction area, the theoretical silicon P_D vs. t approximation (2) shifts downward to [15]:

$$P_D = 110.9\ [t\ (\mu s)]^{-1/2}\ kW/cm^2 \qquad \{Silicon\ 10\ \%\ Hotspot\ Theoretical\} \qquad (4)$$

Similar to the above first-order calculations for silicon rectifiers, theoretical P_D vs. t failure characteristics of 4H-SiC rectifiers can be estimated using basic SiC material properties. While specific heat and thermal conductivity are both functions of temperature, their temperature dependence has not been taken into account in these first-order calculations. Furthermore, there is inconsistency between the few SiC thermal properties that have been reported in the scientific literature. Nevertheless, basic "best-case" and "worst-case" combinations of thermal conductivity and specific heat can be calculated to roughly estimate upper and lower theoretical limits on the junction failure power densities that might be observed in defect-free 4H-SiC junctions. For both calculations, $\rho = 3.2\ gm/cm^3$, $T_i = 298$ K, and $T_m = T_D = 1120$ K [16] were used. The worst-case specific heat $C_p = 0.3$ J/gm-K at 300 K is calculated using the simple Debye model described by Kittel [17]. A worst-case 4H-SiC thermal conductivity $\kappa = 2$ W/cm-K is chosen based on measurements recently reported in [9]. Combined into relation (1) these worst-case material constants yield P_D vs. t relationship for 4H-SiC of:

$$P_D = 2014\ [t\ (\mu s)]^{-1/2}\ kW/cm^2 \qquad \{SiC\ Worst\ Case\ Theoretical\} \qquad (5)$$

The best-case thermal conductivity $\kappa = 4.9$ W/cm-K was chosen from Slack's measurements of 6H-SiC at 300 K [18]. The work of Zyweitz et. al. [16] suggests that the specific heat of 4H-SiC does not increase much beyond $C_p = 1.0$ J/gm-K at temperatures above 600 K. Using these thermal parameters, the best-case first-order estimation of P_D vs. t becomes:

$$P_D = 5755\ [t\ (\mu s)]^{-1/2}\ kW/cm^2 \qquad \{SiC\ Best\ Case\ Theoretical\} \qquad (6)$$

Theoretical relations (2) through (6) are plotted in Figure 2 for reference to experimental data presented in the following section.

EXPERIMENT

Epitaxial mesa-isolated 4H-SiC p^+n junction diodes (n-doping between 2.5×10^{17} to 1.5×10^{18} cm^{-3}) were fabricated on commercial 4H-SiC substrates as previously described in [10]. Nickel annealed at 1000 °C for 5 minutes in an argon tube furnace served as a backside contact, while an unannealed 300 Å Al / 1000 Å Ti / 2000 Å Al sandwich patterned by liftoff provided good ohmic contact to the degenerately doped p^+ cap epilayer.

The presence or absence of screw dislocations in individual devices was conclusively determined by examination of reverse I-V properties as demonstrated in [10]. A total of 17 circular diodes varying in size from 100 μm in diameter to 250 μm in diameter were pulse-tested to failure in this work, 6 of which contained no elementary screw dislocations. Devices were pulse tested on-wafer in near-dark conditions on a probing station equipped with coaxial probes. For pulse

durations of less than 0.5 μs, the charge-line circuit described in [19] was employed to apply pulses and measure device voltage $V_D(t)$ and current $I_D(t)$ transient response. Longer bias pulses were supplied by a Velonex Model 350 pulse generator. Devices were subjected to manually triggered single-shot pulses of increasing pulse amplitudes and/or widths until device failure occurred. Between pulses, device I-V was checked for degradation using a standard 60 Hz curve-tracer. Device failure was observed by sudden changes in the $I_D(t)$ and $V_D(t)$ response, degradation in the curve-tracer measured I-V, and physical changes in device appearance observed with the probe station microscope. Devices were sometimes tested immersed in Fluorinert FC-77 [20] to reduce the possibility of edge-related surface flashover [21], while others were tested in air.

Post-failure optical microscopic examination was carefully conducted on each damaged device. A few devices exhibited clear evidence of surface flashover failure near the mesa periphery. A few devices were totally obliterated similar to what is depicted in [22]. However, strong evidence of bulk junction failure was seen in the majority of diodes tested, as physical contact and mesa damage was confined to near-central regions of the device mesa away from the mesa edge and often away from where the probe tip contacted the diode.

Figure 1 shows $V_D(t)$ and $I_D(t)$ traces of a typically observed device failure on a 200 μm diameter device that contained screw dislocations and was tested immersed in Fluorinert. For the first 0.05 μs of the pulse, the device exhibits negative temperature coefficient of breakdown voltage (NTCBV) behavior, as $I_D(t)$ shows an initial increase while $V_D(t)$ shows an initial decrease. However, the trend reverses to PTCBV behavior, as $I_D(t)$ decreases and $V_D(t)$ increases as the device self heats beyond 0.2 μs into the pulse. Thus, a major experimental finding of this work is that 4H-SiC p^+n junction diodes containing elementary screw dislocations can exhibit PTCBV behavior.

At t = 0.44 μs, the device fails as evidenced by the onset of a sharp current increase coupled with voltage collapse prior to the falling edge of the 0.5 μs bias pulse. Curve-tracer characterization immediately following the pulse confirmed the device failed to a resistive short-circuit during the Figure 1 pulse. An average device power density P_D was calculated by averaging $P(t) = V_D(t)\, I_D(t)$ over the pulse prior to failure and dividing by the total junction area. Thus the device withstood an average power density P_D of 4.17 MW/cm^2 over a period of 0.44 μs in Figure 1, which is one of

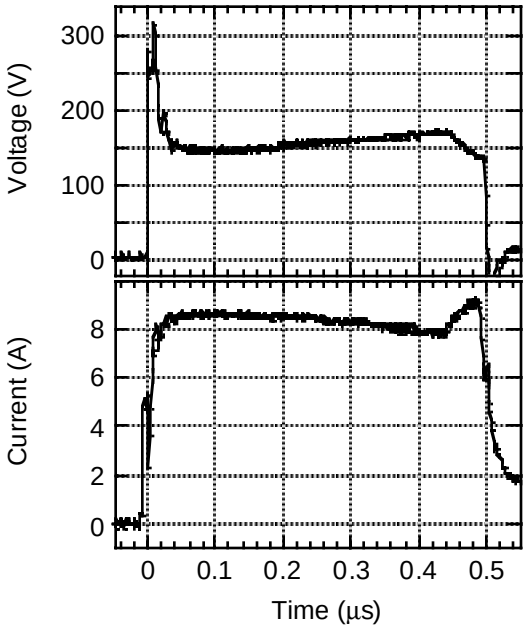

Figure 1: Diode voltage $V_D(t)$ and current $I_D(t)$ transients recording the failure of a 200 μm diameter 4H-SiC p^+n diode under pulse-breakdown testing. The diode fails at 0.44 μs, prior to the falling edge of the 0.5 μs bias pulse.

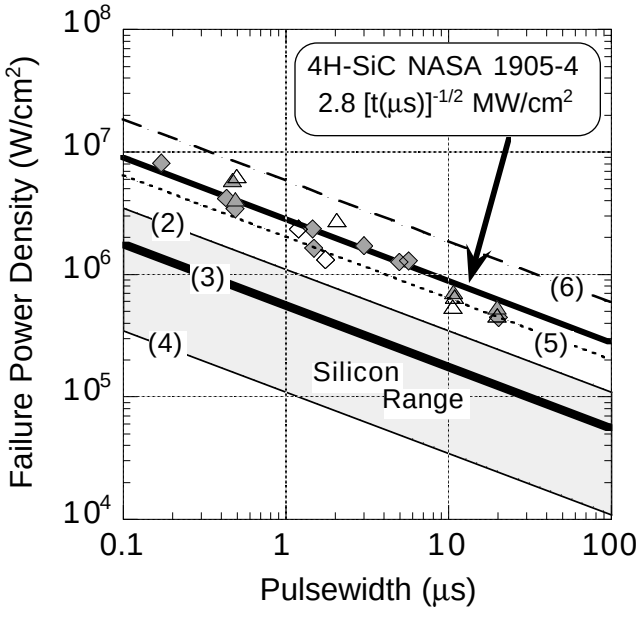

Figure 2: Average power density P_D vs. pulse bias duration t for device reverse breakdown failure. Experimental data points for NASA 4H-SiC p^+n diode sample 1905-4 are plotted along with calculated approximations (2), (3), & (4) for silicon and (5) & (6) for 4H-SiC discussed in the main text.

the experimental data points plotted in Figure 2. Post-failure analysis of this device indicated physical damage in the near-central device region, with no evidence of edge-related breakdown failure.

Figure 2 shows all experimentally P_D vs. t failure data points collected in this study on devices whose DC-measured breakdown voltages ranged from 70 V to 220 V due to n-layer doping variation across the wafer. Diamond symbols on the plot represent devices that clearly exhibited bulk failure where exact failure times and power densities could be directly inferred from the $V_D(t)$ and $I_D(t)$ traces. Triangles represent data points that were collected from pulses in which a diode did not fail (failure occurred during a subsequent pulse), or from pulses where the diode failure occurred at the edge of a device mesa presumably due to surface flashover. Devices that contained no screw dislocations are denoted by open symbols, while filled symbols represent data collected from devices that contained at least one screw dislocation.

The experimentally observed failure data points plotted in Figure 2 are consistent with the $t^{-1/2}$ behavior predicted by Relation (1). The fit to the experimental data:

$$P_D = 2800\ [t\ (\mu s)]^{-1/2}\ kW/cm^2 \qquad \{4H\text{-}SiC\ Experimental\} \qquad (7)$$

falls between the theoretical 4H-SiC limits approximated in (5) and (6). Thus, these 4H-SiC parts can withstand pulse breakdown power densities approximately 5 times the power density that silicon diodes typically withstand before junction failure is reached. It is important to note that this preliminary data indicates that the presence or absence of elementary screw dislocations from a diode had no significant impact on the reverse failure energy of these low-voltage 4H-SiC diodes. Devices with and without screw dislocations exhibited comparable failure power densities to within the range of experimental scatter shown in Figure 2.

CONCLUSION

The presence of elementary screw dislocations did not significantly affect the failure properties of low-voltage (< 250 V) 4H-SiC p^+n junction diodes when subjected to non-adiabatic breakdown-bias pulses. Diodes with and without elementary screw dislocations exhibited positive temperature coefficient of breakdown voltage and high junction failure power densities well above the failure power densities exhibited by highly reliable silicon power rectifiers. This preliminary result, based on measurements from one wafer of 4H-SiC p^+n diodes, suggests that highly reliable low-voltage SiC rectifiers may be attainable in diodes that contain elementary screw dislocations. However, further studies are needed to ascertain the impact of screw dislocations on the failure properties of 4H- and 6H-SiC Schottky rectifiers, high-voltage (> 1 kV) p^+n rectifiers, and other SiC device structures with significant bipolar gain such as thyristors and IGBT's.

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